Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1 OUT**
2. **1 IN-**
3. **1 IN+**
4. **VDD**
5. **2 IN+**
6. **2 IN-**
7. **2 OUT**
8. **3 OUT**
9. **3 IN-**
10. **3 IN+**
11. **GND**
12. **4 IN+**
13. **4 IN-**
14. **4 OUT**

**.068”**

**108”**

**1 2 3 4 5 6 7**

**14 13 12 11 10 9 8**

**MASK**

**REF**

**TLC274F**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: TLC274F**

**APPROVED BY: DK DIE SIZE .068” X .108” DATE: 4/27/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: TLC27L9**

**DG 10.1.2**

#### Rev B, 7/1